

METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

5 Field of the invention

The present invention relates to a method for driving a liquid crystal display, and more particularly to a method for driving a liquid crystal display, in which the response speed of a liquid crystal is improved by the change of gate pulse 10 voltage in an Active Matrix Liquid Crystal Display (hereinafter referred to AM-LCD).

Description of the Prior Art

As generally known in the art, an AM-LCD is an OA (Office Automation) based product for notebooks or monitors developed for word processing or CAD (Computer-aided design) designing on a freeze frame. Recently, with the development of display devices and an increase of requirements for multimedia environment, a clear moving picture has been 20 required in AM-LCD adapted notebooks and monitors, etc. Also, as a digital broadcast becomes widely spread, the demand for AV (Audiovisual) LCD products has been on the rise.

However, an AM-LCD in the prior art adapts a hold-type

driving method for holding displayed data signals for only one field (frame), causing a problem in that a moving picture can not be displayed naturally, unlike an impulsive type CRT (Cathode-ray tube).

5 For instance, in a case where an AM-LCD is driven at 60Hz, signals are held for 1/60 second so that, even an liquid crystal with so rapid response speed is used, the signal level is held every 1/60 second, thus transmitting a moving picture which appears choppy.

10 FIG. 1 is a timing diagram of the conventional AM-LCD according to its driving.

Referring to FIG. 1, in the driving method of the conventional AM-LCD, vertical start signals STV are enabled in 1 vertical period 1V (1V corresponds 16.7ms when driven at 15 60Hz), are synchronized with a transition of vertical clock signal CPV, generating gate pulse voltage, i.e., gate high pulse voltage Vgh and gate low pulse voltage Vgl, thus sequentially scanning the plural gate lines. Herein, V_{syn} which is not described above represents a vertical 20 synchronous signal, and G1~G768 represent drive signals sequentially applied to from 1st gate line to 768th gate line.

FIGs. 2A and 2B are waveform diagrams showing properties of pixel charge/discharge of the conventional AM-LCD, which show pixel charge/discharge properties in a positive field

and a negative field, respectively.

Referring to FIG. 2A, in the positive field, while gate high pulse voltage V_{gh} is outputted at a gate drive IC, TFT channels are opened, electric charges supplied through the 5 data lines are introduced into the pixels, charging the corresponding pixels (1H period). Herein, the period on which electric charges are introduced is called a charge period.

Meanwhile, at the gate drive IC, while gate low pulse 10 voltage V_{gl} is outputted, TFT channels are closed, and applied pixel voltage is reduced by kickback voltage $V_p(+)$, being maintained at a constant level relatively higher than the common voltage V_{com} (1V-1H period). Herein, the period over which electric charges are held is called a holding 15 period.

Referring to FIG. 2B, in the negative field, while gate high pulse voltage V_{gh} is outputted, TFT channels are opened, electric charges flow **into** the date lines, and the corresponding pixels are discharged. Herein, the period over 20 which electric charges **flow** is called a discharge period.

Meanwhile, at the gate drive IC, while gate low pulse voltage V_{gl} is outputted, TFT channels are closed, pixel voltage applied is reduced by kickback voltage $V_p(-)$, maintaining at constant level relatively lower than the

common voltage V_{com} (1V-1H period). Herein, the period over which electric charges are held at a constant level by discharge of electric charges is a holding period.

The conventional driving method of AM-LCD has a drawback 5 in that operational features of an LCD are mainly generated in the holding period among the periods of charge, discharge and holding so that, since the holding period is held for 1V, a stepping phenomenon is generated when providing moving picture, which makes it difficult to reproduce a smooth 10 moving picture.

Also, the driving method of the conventional AM-LCD holds the holding period of gate pulse voltage for up to the next 1 vertical period after generation of gate pulse voltage, which causes a blurring phenomenon that profiles of 15 picture images are blurred. It has been known that this blurring phenomenon is generated when response time of the liquid crystal is long.

SUMMARY OF THE INVENTION

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Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a driving method for LCD which reduces a holding period of gate

pulse voltage, generates gate pulse voltage of multi-level in which pixel voltage converges the common voltage level so as to drive a liquid crystal, thus providing a smooth moving picture.

5 In order to accomplish this object, there is provided a method for driving an LCD in which gate lines are sequentially scanned in 1 vertical period, the method comprising the steps of: sequentially generating a plurality of gate pulse voltages having 1st to 3rd levels while being 10 synchronized with vertical clock signal in said 1 vertical period; in invert driving, dividing the generating period of the plural gate pulse voltages into a charge period, a holding period and a discharge period in respective polar periods corresponding to the 1st to 3rd levels of the plural 15 gate pulse voltage; and converging pixel voltage of the discharge period to a common voltage level, wherein the 3rd level exists in a range between the 1st level and the 2nd level.

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BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the

accompanying drawings, in which:

FIG. 1 is a timing diagram of the conventional AM-LCD according to its driving;

FIGs. 2A and 2B are waveform diagrams showing properties 5 of pixel charge/discharge of the conventional LCD;

FIG. 3 is a view for explaining a driving method of an LCD according to the present invention;

FIG. 4 is a timing diagram for explaining a driving method of an LCD according to the present invention;

10 FIG. 5 is a timing diagram showing relationship between gate pulse voltage and data voltage according to the present invention; and

FIGs. 6A and 6B are waveform diagrams showing properties of pixel charge/discharge of an LCD according to the present 15 invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a preferred embodiment of the present 20 invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description of the same or similar components will be

omitted.

FIG. 3 is a view for explaining a driving method of an LCD according to the present invention, in which only one pixel is shown for easy understanding of the present 5 invention.

Referring to FIG. 3, an AM-LCD comprises a gate line 10 for applying gate pulse voltage, a data line 20 intersecting the gate line 10 for applying pixel voltage, and a thin film transistor (TFT) arranged in a matrix form at the 10 intersecting region of the gate line 10 and the data line 20. In order to drive an AM-LCD, gate pulse voltages as a gate input are generated in which 1st, 2nd and 3rd levels (Vgh, Vgl and Vgl') are provided, and data voltage as a data input is applied to the gate line 10.

15 According to the present invention, the 3rd level Vgl' preferably exists in a range of the 1st level Vgh and the 2nd level Vgl.

FIG. 4 is a timing diagram for explaining a driving method of an LCD according to the present invention.

20 In the driving method of the present invention, vertical start signals STV are enabled in 1 vertical period 1V (1V corresponds to 16.7ms when driven at 60Hz), are synchronized with a transition of vertical clock signal CPV, generating gate pulse voltage having a first, second and third levels

V_{gl}, V_{gh} and V_{gl'}, thus sequentially scanning the plural gate lines. Herein, V_{syn} is vertical synchronous signal and G1~G768 are drive signals sequentially applied to from 1st gate line to 768th gate line.

5 Meanwhile, in order to drive an LCD in a positive field, the period from generation point of gate pulse signal to point where pixel voltage converges the level of common voltage is divided into a charge period, a holding period and a discharge period, and gate pulse voltage with the 1st to 3rd levels V_{gh}, V_{gl} and V_{gl'} is generated corresponding to the
10 respective periods.

Meanwhile, in order to drive an LCD in a negative field, the period from generation point of gate pulse signal to point where pixel voltage converges the level of common voltage is divided into a **charge period**, a holding period and a **discharge period**, and gate pulse voltage with the 1st to 3rd levels V_{gh}, V_{gl} and V_{gl'} is generated corresponding to the respective periods.

FIG. 5 is a timing diagram showing a relationship
20 between gate pulse voltage and data voltage according to the present invention.

As shown in FIG. 5, when the polarity of data voltage is changed, since gate pulse voltage can converge common voltage effectively if the 2nd level of gate pulse voltage V_{gl} is

changed into the 3rd level of gate pulse voltage **Vgl'** after 2n*1H after input of the 1st level of gate pulse voltage Vgh, adapting timing of the 3rd level of gate pulse voltage Vgl' is preferably limited such as 't1=1V-1H-t0=2n*1H, where 0 is 5 positive integer'. That is to say, the holding period of gate pulse voltage preferably maintains 2H..

FIGs. 6A and 6B are the diagrams of waveforms on properties of pixel charge/discharge of an LCD according to the present invention, in which FIG. 6A shows the features of 10 pixel charge/discharge in the positive field and FIG. 6B shows the features of pixel charge/discharge in the negative field.

The driving method of the present invention in the positive field is now described with reference to FIG. 6A.

15 First, if the first level Vgh of gate pulse voltage is generated at a gate drive IC, channels of TFT are opened in a period in which the first level Vgh is maintained. At this point, when data voltage Vdata(+) is applied at a source drive IC, a pixel electrode has an increased charge level 20 while electric charges are introduced into the pixel electrode, charging the electrode in a charge period in which the first level Vgh is maintained.

At this state, when gate pulse voltage is transited from the first level Vgh to the second level Vgl, pixel voltage is

reduced by kickback voltage $V_p(+)$ and thus maintained constantly in the holding period. Herein, the holding period provided is preferably shorter than the conventional type.

Second, when the third level $V_{gl'}$ of gate pulse voltage 5 is generated after maintaining a certain holding period, channels of TFT are opened again, electric charges introduced into the pixel are escaped, so that pixel voltage $V_{pixel}(+)$ converges the level of common voltage. Herein, the discharge period is preferably set to a range higher than 1 horizontal 10 period 1H but lower than 1 vertical period 1V.

Herein, transition point of the third level $V_{gl'}$ of gate pulse voltage is set according to a response time of the liquid crystal, i.e., rising time and falling time of the liquid crystal. According to an embodiment of the present 15 invention, the rising time of the liquid crystal is above 10ms and the falling time of the liquid crystal is below 5ms.

Meanwhile, according to an embodiment of the present invention, if the holding period is t_1 and the discharge period is t_2 , the holding period t_1 equals $1H-1V-t_2$.

20 The driving method of the present invention in the negative field is now described with reference to FIG. 6B.

First, if the first level V_{gh} of gate pulse voltage is generated at a gate drive IC, channels of TFT are opened in a period in which the first level V_{gh} is maintained. At this

point, when data voltage $V_{data}(+)$ is applied at a source drive IC, a pixel electrode has an increased charge level while electric charges are introduced into the pixel electrode, charging the electrode in a charge period in which 5 the first level V_{gh} is maintained.

At this state, when gate pulse voltage is transited from the first level V_{gh} to the second level V_{gl} , pixel voltage is reduced by kickback voltage $V_p(+)$ and thus maintained constantly in the holding period. Herein, the holding period 10 provided is preferably shorter than the conventional type.

Second, when the third level V_{gl}' of gate pulse voltage is generated after maintaining a certain holding period, channels of TFT are opened again, electric charges are introduced into the pixel electrode, so that pixel voltage 15 $V_{pixel}(-)$ converges the level of common voltage V_{com} . Herein, the discharge period is preferably set to a range, which is higher than 1 horizontal period $1H$ but is lower than 1 vertical period $1V$ like in the positive period.

Herein, transition point of the third level V_{gl}' of gate 20 pulse voltage is set according to a response time of the liquid crystal, i.e., rising time and falling time of the liquid crystal. According to an embodiment of the present invention, the rising time of the liquid crystal is above 10ms and the falling time of the liquid crystal is below 5ms.

Thus, when pixel voltage converges into common voltage, liquid crystal is in a state of free decay during this period, so that data in the pixel is held during the holding period and is changed into black in the converging period by 5 charge/discharge. This means that it is transformed into a normally black mode, reducing response time and thus obtaining picture quality similar to a pulse type. Also, this generates an effect that the change of the picture image locked up upon conversion of a frame is unlocked in the 10 middle of the frame.

Meanwhile, data outputted in each frame converge into a black state after outputting desired video data, and then data of the next frame are outputted and converge into the black state. Accordingly, the present invention can solve 15 problems in picture image processing due to transition between data, such as slow response speed due to the transition into a middle gray level, securing of time for response speed of the liquid crystal after holding, etc.

Also, since pixel voltage converges into Vcom at every 20 frame transition due to the driving of the gate drive IC, fewer electric charges are required in charging or discharging the pixel electrode, thus reducing the quantity of electric charge required to output the source drive IC.

In the driving method of gate pulse voltage according to

the present invention as described above, pixel voltage converges into the level of common voltage in each vertical period, so as to reduce generation of stepping phenomenon, blurring phenomenon, and afterimages, thereby enabling 5 effective realization of moving pictures.

Further, the quantity of electric charge is reduced so that power consumption is reduced. Accordingly, capacitance between the gate and the source generated by overlapping of the TFT gate line and data line is reduced, thus preventing 10 degradation of display property due to the coupling.

Although preferred embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing 15 from the scope and spirit of the invention as disclosed in the accompanying claims.